AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

1. (Previously presented): A semiconductor device, comprising:

a substrate;

a first multilayer interconnection structure formed over said substrate; and

a second multilayer interconnection structure formed over said first multilayer interconnection structure,

wherein said first multilayer interconnection structure includes a first interlayer insulation film and a first interconnection layer included in said first interlayer insulation film;

said second multilayer interconnection structure includes a second interlayer insulation film and a second interconnection layer included in said second interlayer insulation film,

said first multilayer interconnection structure including a pillar vertically extending straight from a surface of said substrate and reaching at least said second multilayer interconnection structure, said pillar being formed in a region of said substrate right underneath an electrode pad so as to support stress during wire bonding,

said first interconnection layer being formed so as to avoid said pillar, and

said pillar being provided on a device isolation structure on said substrate,

wherein said first interlayer insulation film has a first Young modulus and said second interlayer insulation film has a second, larger Young modulus than said first Young modulus.

2. (Original): The semiconductor device as claimed in claim 1, wherein said pillar has a layered structure identical to a layered structure of said first interconnection layer in said first multilayer interconnection structure.

3. (Withdrawn): The semiconductor device as claimed in claim 1, wherein said pillar has a composition different from a composition of said first interconnection layer in said first multilayer interconnection structure.

4. (Original): The semiconductor device as claimed in claim 1, wherein said pillar has an edge part engaging to a bottom surface of said second multilayer interconnection structure.

5. (Original): The semiconductor device as claimed in claim 1, wherein said pillar extends further in said second multilayer interconnection structure and has a layered structure identical to a layered structure of said second interconnection layer in a part thereof extending in said second multilayer interconnection structure.

6. (Withdrawn): The semiconductor device as claimed in claim 1, wherein said pillar extends further in said second multilayer interconnection structure, and wherein said pillar has a composition different from a composition of said first and second interconnection layers.

7. (Original): The semiconductor device as claimed in claim 1, wherein an electrode pad is formed on said second multilayer interconnection structure.

8. (Previously presented): The semiconductor device as claimed in claim 7, wherein said pillar is formed in plural numbers so as to occupy at least 15% of the area of said region of said substrate right underneath said electrode pad as a whole.

9. (Original): The semiconductor device as claimed in claim 7, wherein there is formed an active device in a region of said substrate right underneath said electrode pad.

10. (Cancelled).

11. (Original): The semiconductor device as claimed in claim 10, wherein said first Young modulus has a value less than 30GPa and said second Young modulus has a value equal to or larger than 30GPa.

12. (Original): The semiconductor device as claimed in claim 10, wherein said first Young modulus has a value 1/2 or less of said second Young modulus.

13. (Original): The semiconductor device as claimed in claim 1, wherein said pillar has a Young modulus of 30GPa or more.

14. (Original): The semiconductor device as claimed in claim 1, wherein, in said first multilayer interconnection structure, said pillar is formed with plural numbers so as to be located at both sides of an interconnection pattern forming a part of said first interconnection layer.

15. (Original): The semiconductor device as claimed in claim 1, wherein said pillar forms a wall extending continuously on said surface of said substrate.

16. (Original): The semiconductor device as claimed in claim 1, wherein said pillar extends continuously along a circumference of said substrate in said first and second multilayer interconnection structures and form a guard ring.

17. (Original): The semiconductor device as claimed in claim 1, wherein said first interlayer insulation film is formed of a porous film.

18. (Original): The semiconductor device as claimed in claim 1, wherein said first interlayer insulation film is an organic film.

19. (Original): The semiconductor device as claimed in claim 1, wherein said second interlayer insulation film is a CVD insulation film.

20. (Cancelled).

21. (Original): The semiconductor device as claimed in claim 1, wherein said pillar is provided in plural number on said substrate, and wherein there is formed a reinforcement structure in said first multilayer interconnection structure so as to extend diagonally between said plural pillars.

22. (Withdrawn): A multilayer interconnection structure comprising stacking of at least two interconnection layers with an intervening via-layer,

each of said interconnection layers comprising an interlayer insulation film and an interconnection pattern formed in said interlayer insulation film,

said via-layer comprising a via-interlayer insulation film and a via-plug formed in said via-interlayer insulation film,

said via-plug connecting said interconnection pattern in said interconnection layer located on said via-layer to said interconnection pattern in said interconnection layer located under said via-layer,

said interlayer insulation film forming said via-layer having a smaller film thickness and a larger elastic modulus than any of said interlayer insulation films constituting said interconnection layers on and under said via-layer.

23. (Withdrawn): The multilayer interconnection structure as claimed in claim 22, wherein, in said interconnection layers on and under said via-layer, said interlayer insulation film has a film thickness of less than 300nm.

24. (Withdrawn): The multilayer interconnection structure as claimed in claim 22, wherein said interlayer insulation film constituting said via-layer has a film thickness of about 180nm.

25. (Withdrawn): A semiconductor device comprising

a substrate;

a first multilayer interconnection structure formed on said substrate; and

a second multilayer interconnection structure formed on said first multilayer interconnection structure,

said first multilayer interconnection structure including stacking of at least two interconnection layers with an intervening via-layer,

each of said interconnection layers comprising an interlayer insulation film and an interconnection pattern formed in said interlayer insulation film,

said via-layer comprising a via-interlayer insulation film and a via-plug formed in said via-interlayer insulation film,

said via-plug connecting said interconnection pattern in said interconnection layer located on said via-layer and said interconnection pattern in said interconnection layer located under said via-layer,

said via-interlayer insulation film constituting said via layer having a smaller film thickness and a larger elastic modulus than any of said interlayer insulation films constituting said interconnection layers located on and under said via-layer,

said interconnection pattern in each interconnection layer and said via-plug in each via-layer extending, in said first interlayer insulation film, continuously from said substrate surface through said first multilayer interconnection structure and forming a pillar at least reaching said second multilayer interconnection structure.

26. (Withdrawn): A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

a plurality of pillars being formed in said multilayer interconnection structure so as to reach a surface of said substrate;

a reinforcement structure being formed in said multilayer interconnection structure diagonally among said plurality of pillars.

27. (Withdrawn): A semiconductor device as claimed in claim 26, wherein there is formed another multilayer interconnection structure on said multilayer interconnection structure,

and wherein said multilayer interconnection structure includes an interlayer insulation film having a specific dielectric constant lower than a specific dielectric constant of an interlayer insulation film in said another multilayer interconnection structure provided thereon.

28. (Withdrawn): The semiconductor device as claimed in claim 26, wherein said reinforcement structure has a layered structure identical to a layered structure of said interconnection layer in said multilayer interconnection structure.

29. (Previously presented): The semiconductor device as claimed in claim 1, wherein said pillar is formed of a plurality of segments aligned straight from said device isolation structure to said contact pad.

30. (Previously presented): The semiconductor device as claimed in claim 1, wherein said pillar engages with a bottom surface of said contact pad via a plug formed in a passivation film.